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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,495	02/20/2004	Yung-Cheng Chen	N1085-00251 [TSMC2003-083	2148

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DUANE MORRIS LLP
IP DEPARTMENT (TSMC)
30 SOUTH 17TH STREET
PHILADELPHIA, PA 19103-4196

EXAMINER	
NORTON, JENNIFER L	

ART UNIT	PAPER NUMBER
2121	

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/783,495	CHEN ET AL.	
	Examiner	Art Unit	
	Jennifer L. Norton	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2/20/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 are pending.

Claim Objections

2. Claims 5, 7-8, 12, 14-18, and 21-22 are objected to because of the following informalities:

a. Claim 5 includes the abbreviation CMP in line 2.

b. Claim 7 includes the abbreviation CD in line 2.

c. Claim 8 includes the abbreviation CD in line 4.

d. Claim 12 includes the abbreviation CD in line 6.

e. Claim 14 includes the abbreviation CD in line 1.

f. Claim 15 includes the abbreviation CD in line 4.

g. Claim 16 includes the abbreviation STI in line 2.

h. Claim 17 includes the abbreviation CD in line 1.

i. Claim 18 includes the abbreviations STI in line 2 and CD in line 4.

j. Claim 21 includes the abbreviation STI in line 2.

k. Claim 22 includes the abbreviation CD in line 1.

There is no reference to the definition of the abbreviations in any supporting claims for the claims given above. All abbreviations should be spelled out in the claims to avoid any question of ambiguity.

Appropriate correction is required.

3. Claim 12 is objected to because of the following informalities:

Claim 12, line 5 includes the spelling error of "feed back". "Feedback" should be spelled the same way in all claims to maintain continuity.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-4 and 9-11 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,409,538 (hereinafter Nakayama).

6. As per claim 1, Nakayama discloses a method for controlling exposure energy on a wafer substrate, comprising the steps of:

controlling the exposure energy with a feedback process control signal of critical dimension (col. 6, lines 14-20 and 48-55, col. 15, lines 12-21 and Fig. 18), and

further controlling the exposure energy with a feed forward process control signal of a compensation amount that compensates for wafer thickness variations (col. 6, lines 48-55 and col. 15, lines 17-33).

7. As per claim 2, Nakayama discloses combining the feed forward control signal with the feedback process control signal to control the exposure energy (col. 15, lines 14-33 and Fig. 18).

8. As per claim 3, Nakayama discloses supplying the feed forward process control signal by a feed forward controller (col. 15, lines 21-33 and Fig. 18, element 45).

9. As per claim 4, Nakayama discloses controlling the exposure energy by a feed forward control signal of an interlayer thickness measurement (col. 6, lines 48-55, col. 15, lines 8-28 and Fig. 18, element 56).

10. As per claim 9, Nakayama discloses calculating the compensation amount according to a polynomial function with higher order coefficients set at zero (col. 5, lines 17-32 and 38-51).

11. As per claim 10, Nakayama discloses calculating the compensation amount according to a linear function (col. 5, lines 38-51).

12. As per claim 11, Nakayama discloses calculating the compensation amount according to a segmented linear function (col. 5, lines 17-32 and 38-51).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 5-8 and 12-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama in view of U.S. Patent No. 6,798,529 (hereinafter Saka).

15. As per claim 5, Nakayama teaches controlling the exposure energy by a feed forward control signal of an interlayer thickness measurement (col. 15, lines 8-28 and Fig. 18, element 56).

Nakayama does not expressly teach an interlayer thickness measurement remaining after CMP.

Saka teaches to an interlayer thickness measurement remaining after CMP (col. 8, lines 61-63 and col. 13, lines 27-33).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Nakayama to include an

interlayer thickness measurement remaining after CMP to continuously and in-situ, monitor localized regions of a wafer surface during the CMP process (col. 5, lines 38-40).

16. As per claim 6, Nakayama teaches calculating the compensation amount according to a polynomial function with a coefficient of the function being based on a measurement of a thickness of a planarized interlayer (col. 6, lines 35-55 and col. 15, lines 17-33).

Nakayama does not expressly teach a measurement of a remaining thickness of a planarized interlayer.

Saka teaches to a measurement of a remaining thickness of a planarized interlayer (col. 8, lines 61-63 and col. 13, lines 27-33).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Nakayama to include a measurement of a remaining thickness of a planarized interlayer to continuously and in-situ, monitor localized regions of a wafer surface during the CMP process (col. 5, lines 38-40).

17. As per claim 7, Nakayama teaches to calculating the feedback process control signal of CD measurement of a layer (col. 6, lines 48-55, col. 15, lines 21-33 and Fig. 18)

Nakayama does not expressly teach calculating the feedback process control signal of CD measurement of a top layer in a previous manufacturing lot.

Saka teaches to calculating the feedback process control signal of CD measurement of a top layer in a previous manufacturing lot (col. 12, lines 32-35).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Nakayama to include calculating the feedback process control signal of CD measurement of a top layer in a previous manufacturing lot to continuously and in-situ, monitor localized regions of a wafer surface during the CMP process (col. 5, lines 38-40).

18. As per claim 8, Nakayama teaches to calculating the compensation amount according to a polynomial function with a coefficient of the function being based on a measurement of a remaining thickness of a planarized interlayer (col. 6, lines 48-55) and calculating the feedback process control signal of CD measurement of a layer (col. 15, lines 17-33).

Nakayama does not expressly teach a CD measurement of a top layer in a previous manufacturing lot.

Saka teaches to a CD measurement of a top layer in a previous manufacturing lot (col. 6, lines 58-60, col. 9, lines 28-33 and col. 12, lines 32-35).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Nakayama to include a CD measurement of a top layer in a previous manufacturing lot to continuously and in-situ, monitor localized regions of a wafer surface during the CMP process (col. 5, lines 38-40).

19. As per claim 12, Nakayama teaches a system for controlling exposure energy on a wafer substrate, comprising:

a feed forward controller (Fig. 18, element 45) providing a feed forward control signal to an exposure apparatus based on a thickness measurement of an interlayer of the wafer substrate for controlling the exposure energy focused on a top layer of the wafer substrate (col. 15, lines 17-33), and

a feed back controller (Fig. 18, element 45) providing a feed back exposure energy control signal to the exposure apparatus based on CD measurement of a layer of a wafer substrate (col. 17-33).

Nakayama does not expressly teach a CD measurement of a top layer of a wafer substrate of a previous manufacturing lot.

Saka teaches to a CD measurement of a top layer of a wafer substrate of a previous manufacturing lot (col. 6, lines 58-60, col. 9, lines 28-33 and col. 12, lines 32-35).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Nakayama to include CD measurement of a top layer of wafer substrates of a previous manufacturing lot to continuously and in-situ, monitor localized regions of a wafer surface during the CMP process (col. 5, lines 38-40).

20. As per claim 13, Nakayama discloses a thickness measurement device (Fig. 18, element 56) providing thickness measurement data to the feed forward controller (col. 15, lines 8-28 and Fig. 18, element 45).

21. As per claim 14, Nakayama discloses a CD measurement device (Fig. 18, element 56) providing CD measurement data to the feedback controller (Fig. 18, element 45 and col. 15, lines 8-28).

22. As per claim 15, Nakayama discloses a thickness measurement device (Fig. 18, element 56) providing thickness measurement data to the feed forward controller (Fig. 18, element 45 and col. 15, lines 8-28) and a CD measurement device (Fig. 18, element 56) providing CD measurement data to the feedback controller (Fig. 18, element 45 and col. 15, lines 8-28).

23. As per claim 16, Nakayama discloses a thickness measurement device (Fig. 18, element 56) providing thickness measurement data of an STI layer of the wafer substrate to the feed forward controller (Fig. 18, element 45 and col. 15, lines 8-28).

24. As per claim 17, Nakayama teaches a CD measurement device (Fig. 18, element 56) providing CD measurement data of a poly-gate of wafer substrates (col. 15, lines 8-17).

Nakayama does not expressly teach to CD measurement data of a poly-gate of wafer substrates of a previous manufacturing lot.

Saka teaches to CD measurement data of a poly-gate of wafer substrates of a previous manufacturing lot (col. 6, lines 58-60, col. 9, lines 28-33 and col. 12, lines 32-35).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Nakayama to include CD measurement data of a poly-gate of wafer substrates of a previous manufacturing lot to continuously and in-situ, monitor localized regions of a wafer surface during the CMP process (col. 5, lines 38-40).

25. As per claim 18, Nakayama teaches to a thickness measurement device providing thickness measurement data of an STI layer of the wafer substrate to the feed forward controller (Fig. 18, element 45 and col. 15, lines 8-17); and

a CD measurement device (Fig. 18, element 56) providing CD measurement data of a poly-gate (col. 15, lines 8-17).

Nakayama does not expressly teach to CD measurement data of a poly-gate of a previous manufacturing lot.

Saka teaches to CD measurement data of a poly-gate of wafer substrates of a previous manufacturing lot (col. 6, lines 58-60, col. 9, lines 28-33 and col. 12, lines 32-35).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Nakayama to include CD

measurement data of a poly-gate of wafer substrates of a previous manufacturing lot to continuously and in-situ, monitor localized regions of a wafer surface during the CMP process (col. 5, lines 38-40).

26. As per claim 19, Nakayama discloses the feed forward controller is user configurable by having one or more polynomial coefficients set to zero in a polynomial function model (col. 5, lines 17-32 and 38-51).

27. As per claim 20, Nakayama discloses the feed forward controller is user configurable by having one or more polynomial coefficients set to zero in a polynomial function model (col. 5, lines 17-32 and 38-51).

28. As per claim 21, Nakayama discloses a system as set forth above, comprising:

a thickness measurement device (Fig. 18, element 56) providing thickness measurement data of an STI layer of the wafer substrate to the feed forward controller (Fig. 18, element 45 and col. 15, lines 8-28).

29. As per claim 22, Nakayama teaches a CD measurement device (Fig. 18, element 56) providing CD measurement data of a poly-gate of wafer substrates (col. 15, lines 8-28).

Nakayama does not expressly teach to measurement data of a poly-gate of wafer a previous manufacturing lot.

Saka teaches to CD measurement data (Fig .6) of a poly-gate of wafer substrates of a previous manufacturing lot (col. 6, lines 58-60, col. 9, lines 28-33 and col. 12, lines 32-35).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Nakayama to include CD measurement data of a poly-gate of wafer substrates of a previous manufacturing lot to continuously and in-situ, monitor localized regions of a wafer surface during the CMP process (col. 5, lines 38-40).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following references are cited to further show the state of the art with respect to manufacturing semi-conductors.

U.S. Patent No. 6,331,488 discloses treatment (i.e. chemical mechanical planarization or etching process) may be used to planarize the layers before subsequent deposition of a layer of material thereover. In this manner, the surface irregularities of a layer may be minimized so that sequent layers deposited thereon do not substantially reflect the irregularities of the underlying layer (col. 1, lines 40-50).

U.S. Patent No.: 5,5747,201 discloses a method for controlling the formation of a thin film for stabilization of formation or treatment of a semi-conductor.

U.S. Patent No.: 6,625,512 discloses a method and apparatus for control of final critical dimensions during the processing of semi-conductor wafers.

U.S. Patent No.: 5,926,690 discloses a control system used in semi-conductor fabrication for controlling critical dimensions.

U.S. Patent Publication No.: 2004/0102857 discloses a method and apparatus for employing a secondary process controller in conjunction with a primary process controller.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer L. Norton whose telephone number is 571-272-3694. The examiner can normally be reached on 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Anthony Knight can be reached on 571-272-3687. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Anthony Knight
Supervisory Patent Examiner
Art Unit 2121